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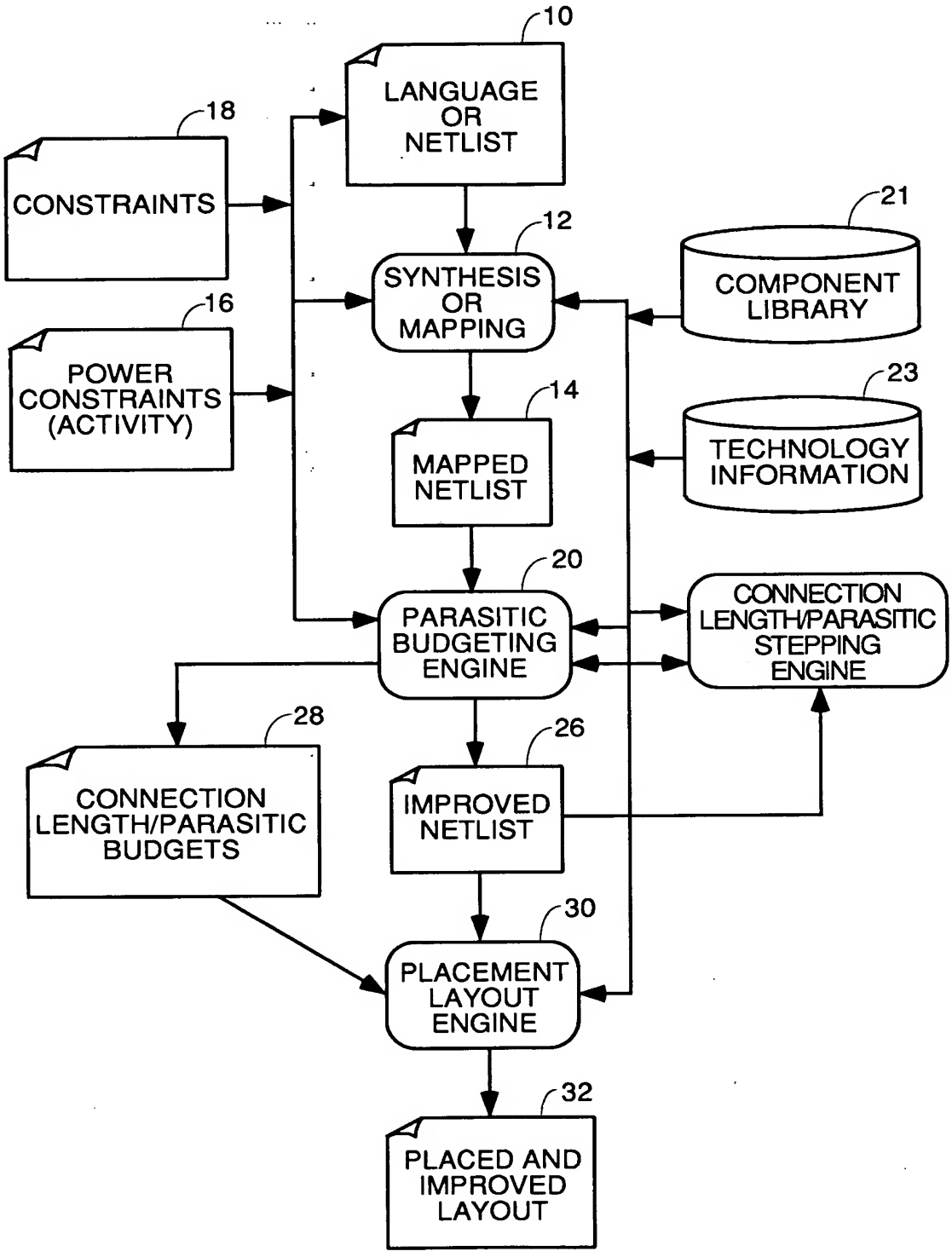
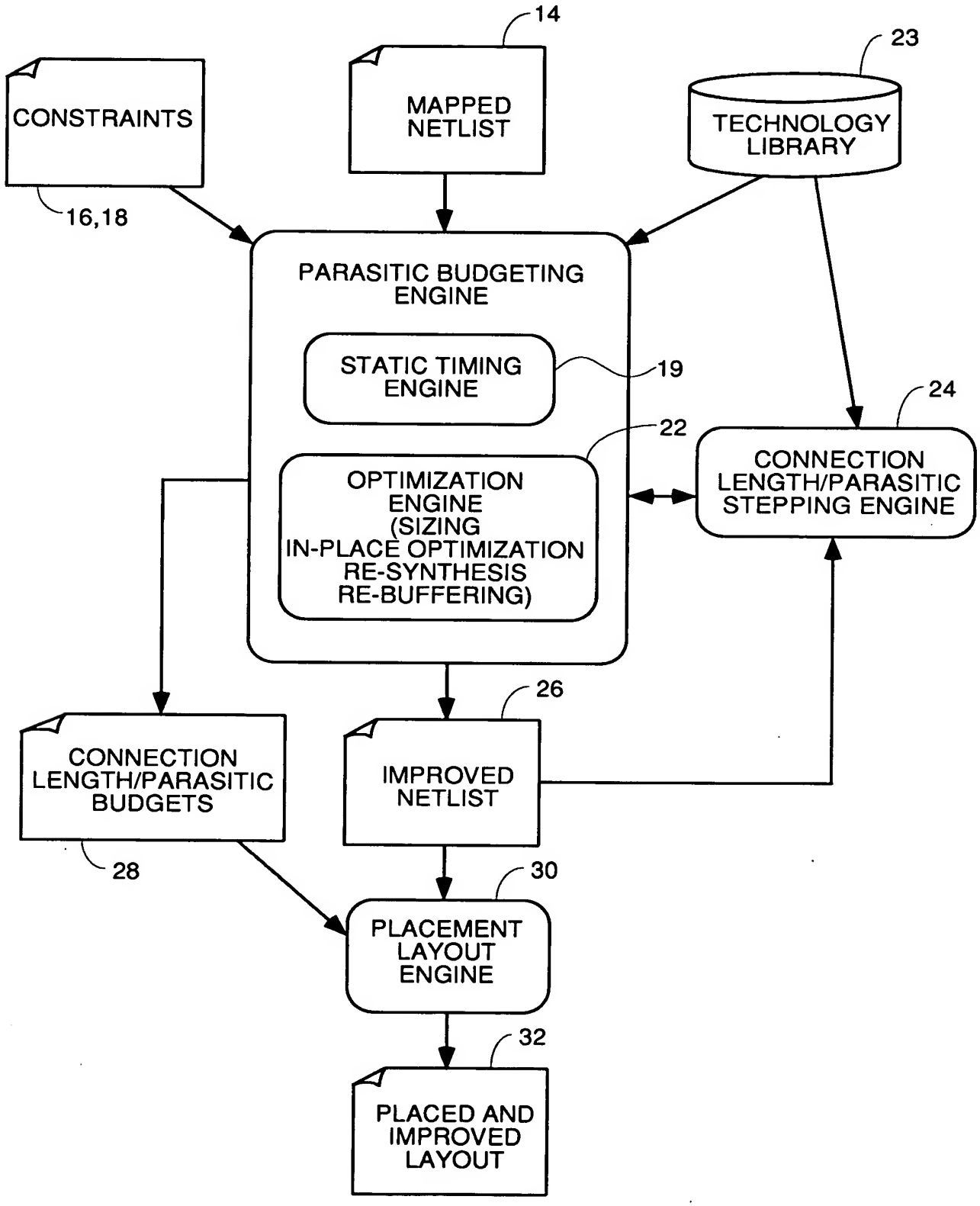
JUL 27 2004
PATENT & TRADEMARK OFFICE



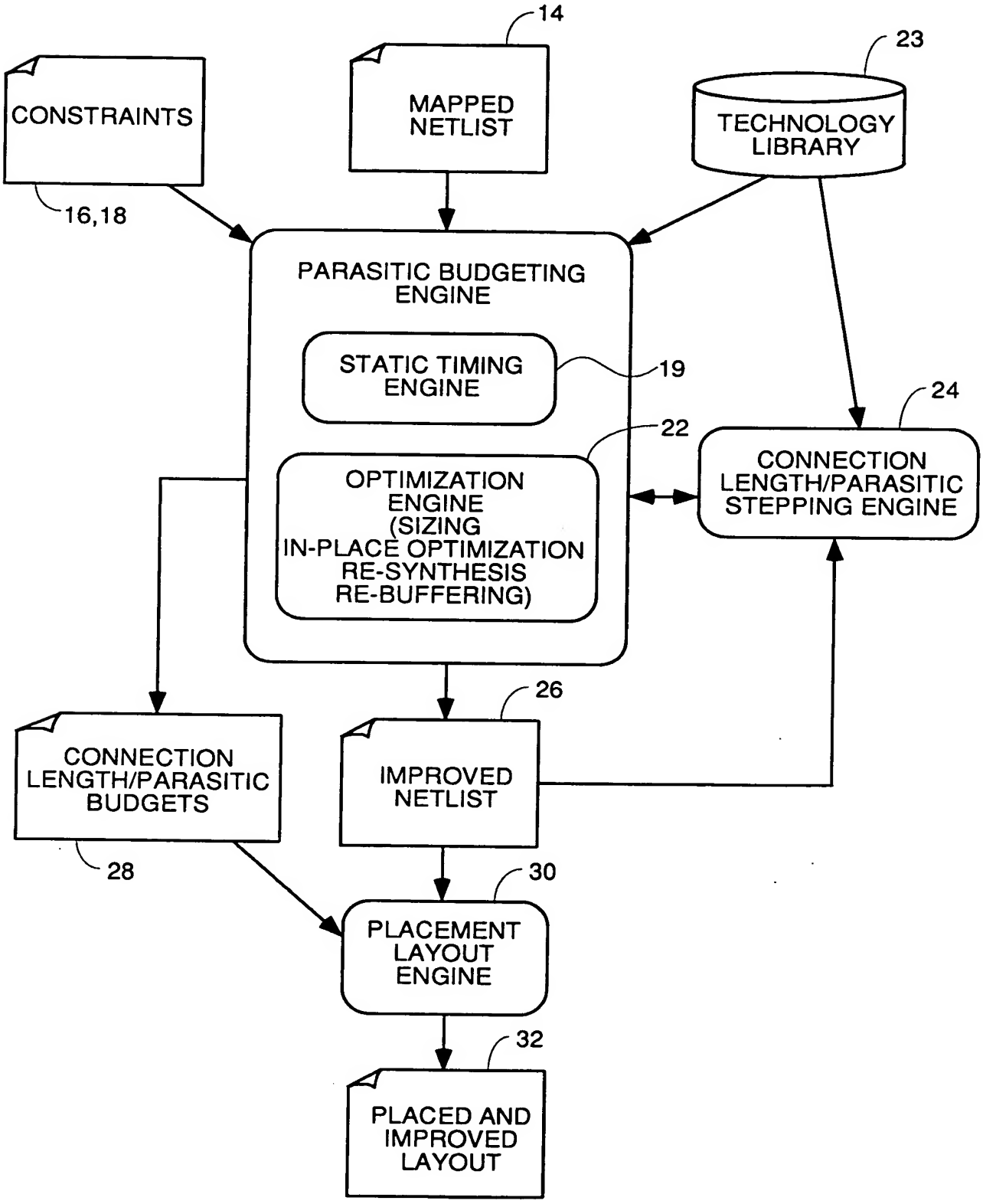
PARASITIC BUDGETING FLOW

FIG. 1



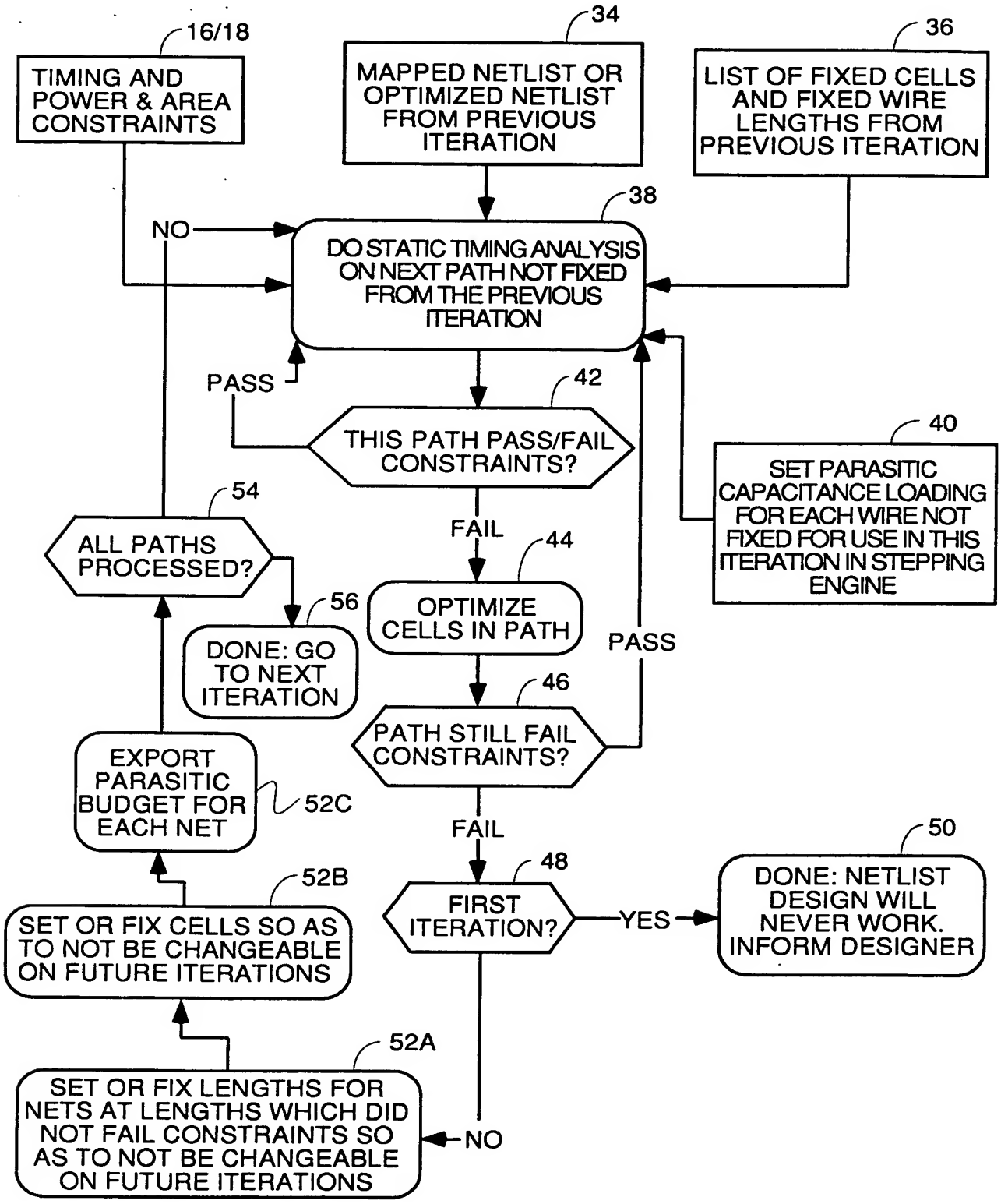
PARASITIC BUDGETING FLOW

FIG. 2A



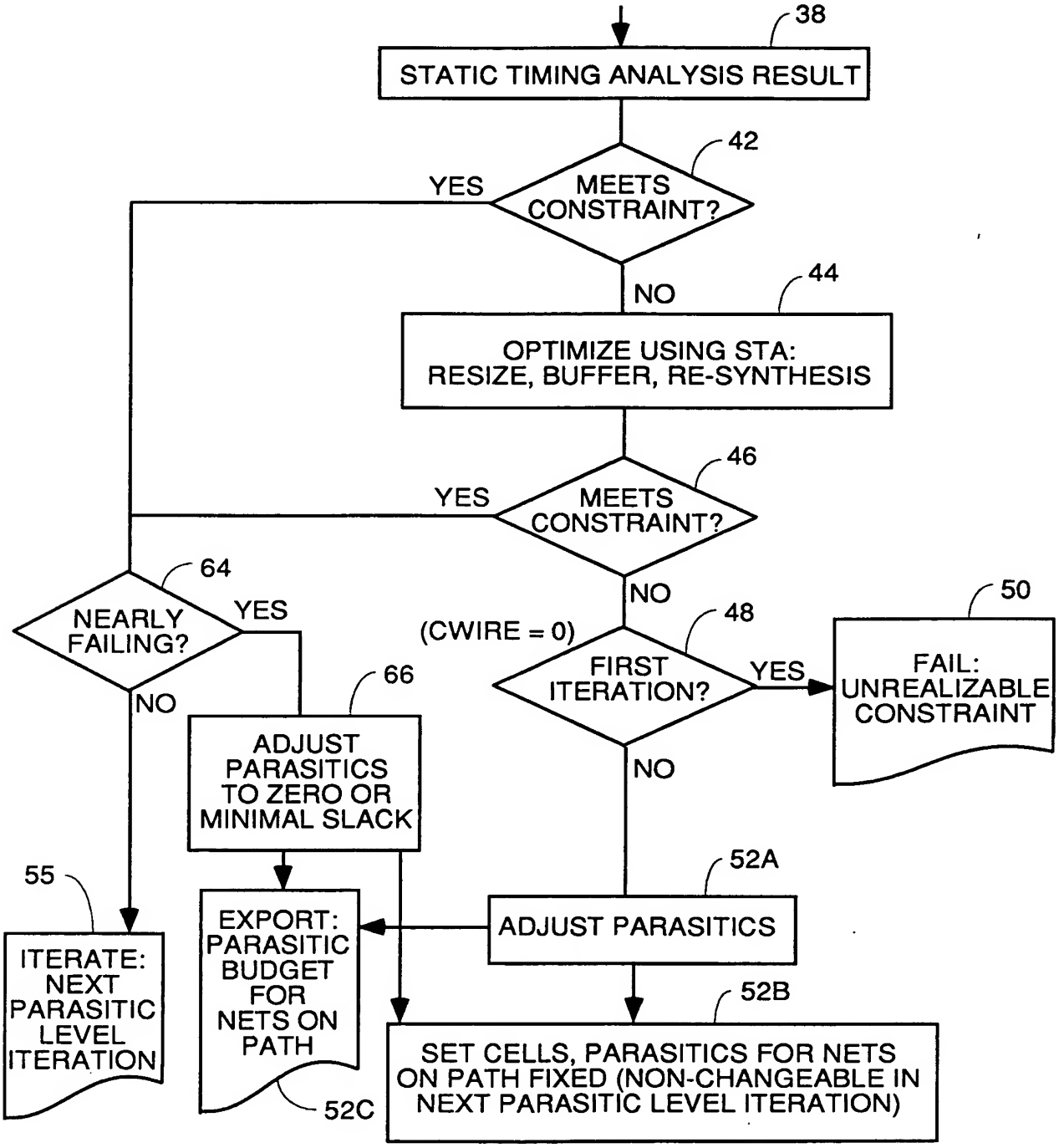
PARASITIC BUDGETING FLOW

FIG. 2A



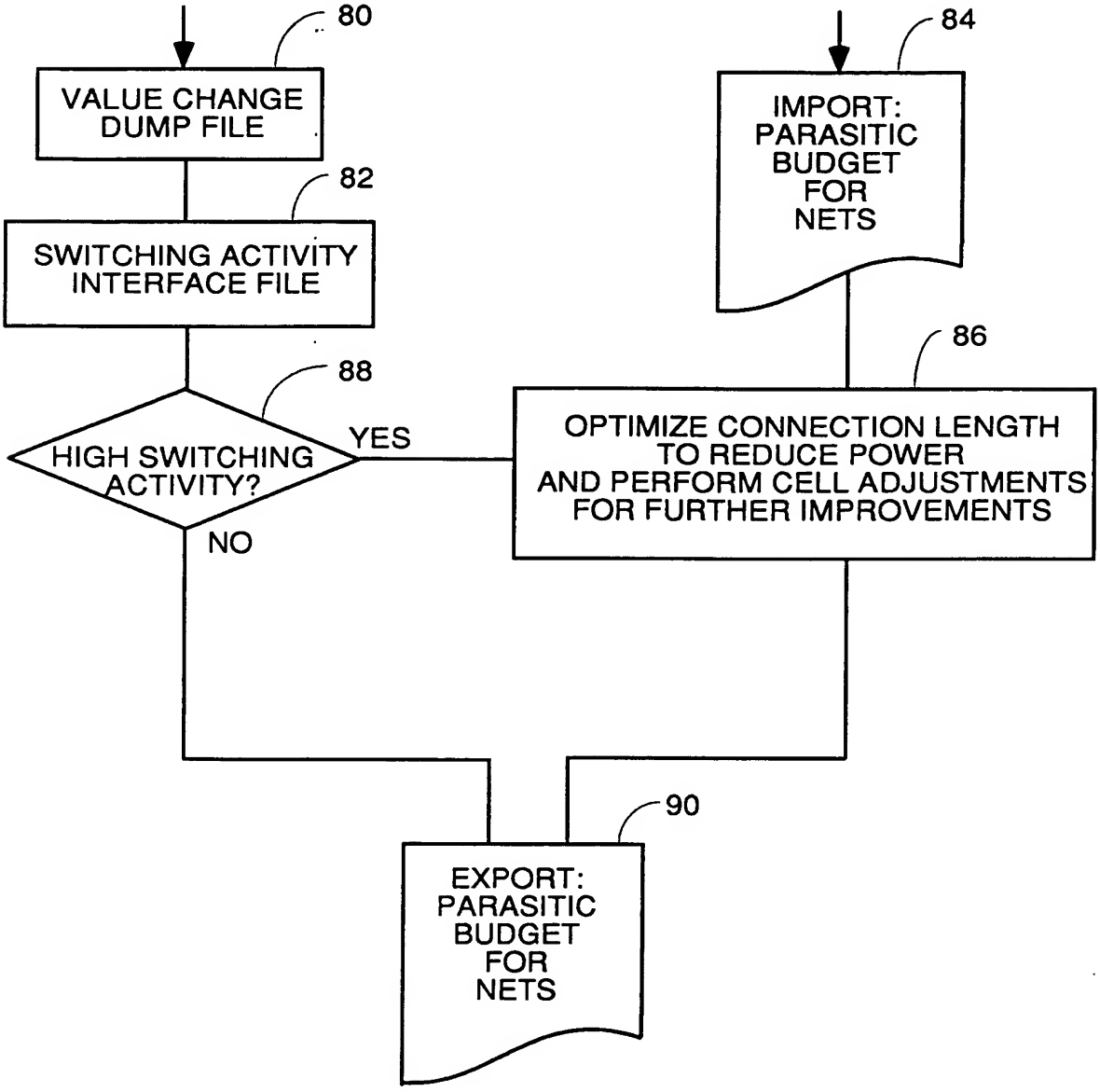
PROCESS FLOW FOR ONE ITERATION OF THE ITERATIVE PARASITIC BUDGET OPTIMIZATION PROCESS

FIG. 2B



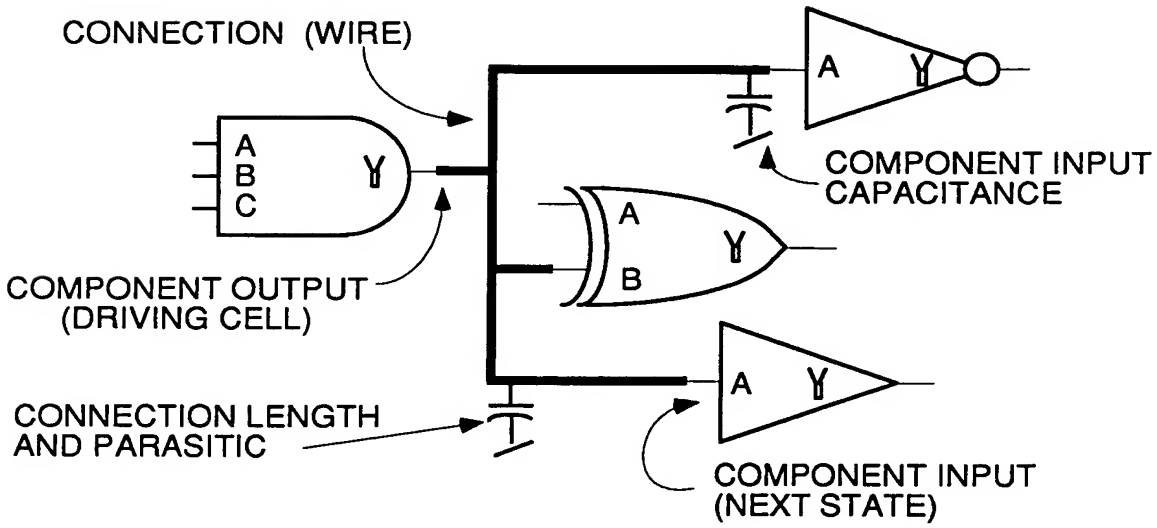
ALTERNATE IMPLEMENTATION FLOW FOR EACH PATH INSIDE EACH PARASITIC LEVEL ITERATION.

FIG. 2C



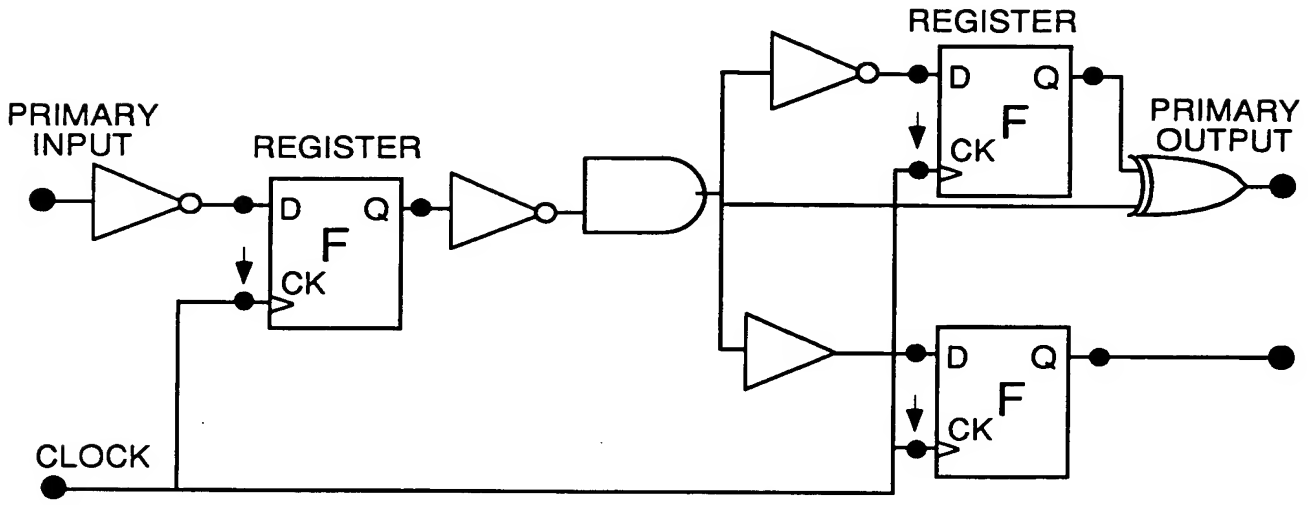
ALTERNATE IMPLEMENTATION FLOW
POWER OPTIMIZATION OF PARASITIC BUDGET

FIG. 2D



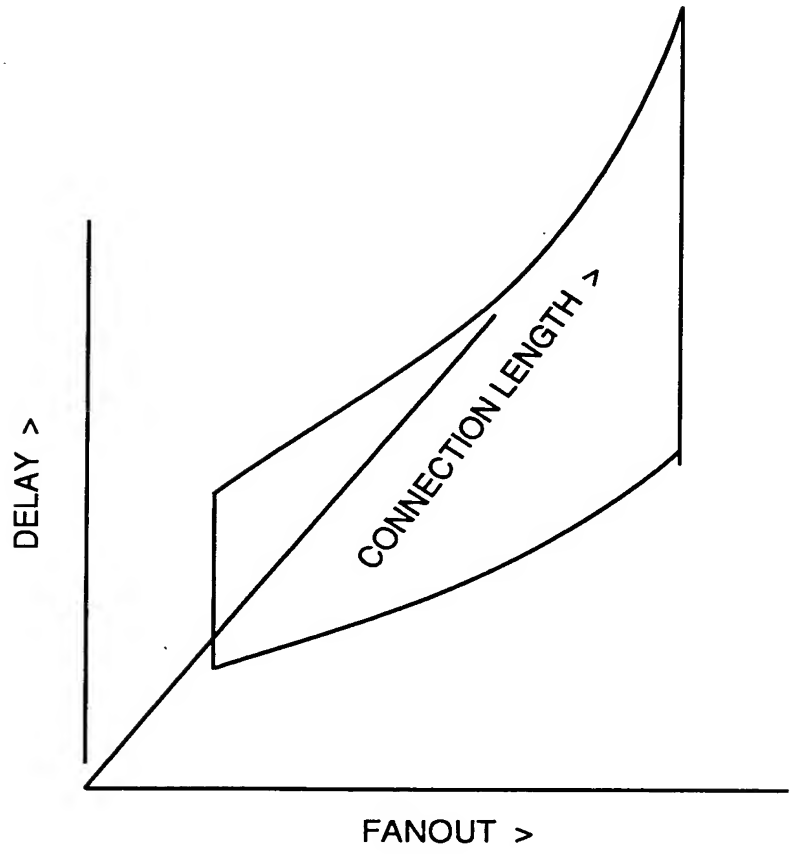
CRITICAL PATH STAGE ELEMENT

FIG. 3



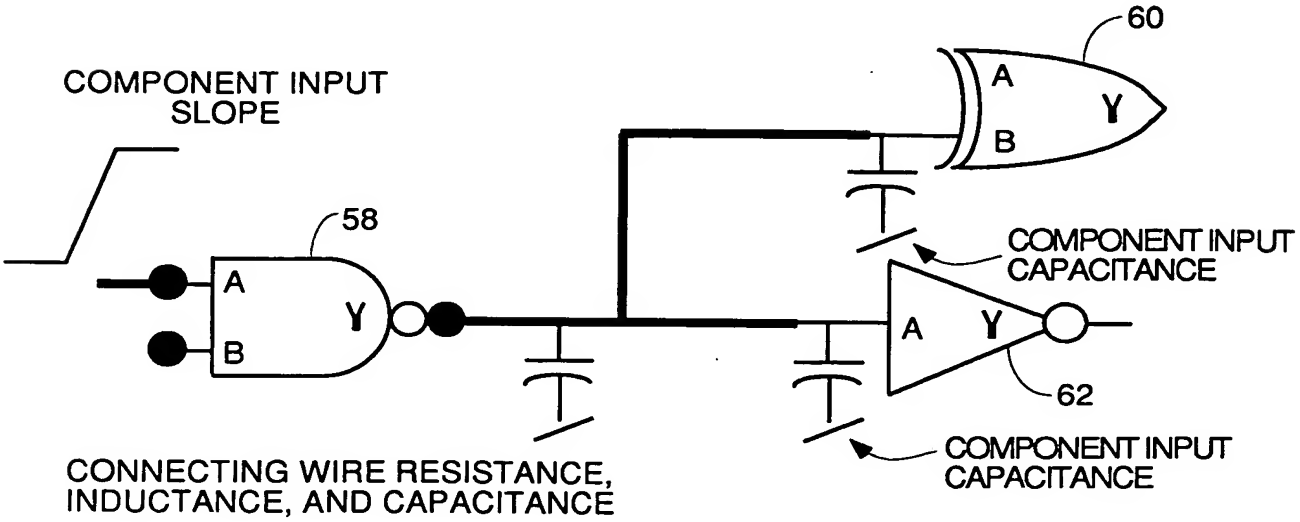
CRITICAL PATH REGISTER STRUCTURE

FIG. 4



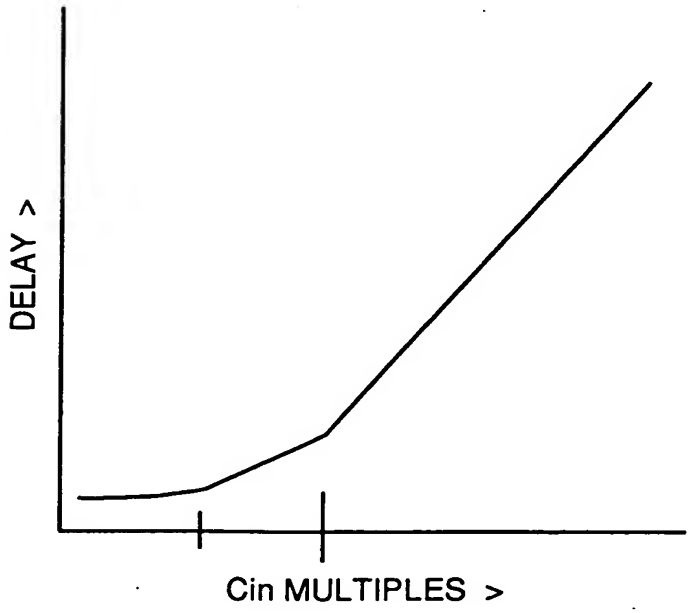
DELAY AS FUNCTION OF FANOUT AND CONNECTION LENGTH

FIG. 5



PARASITIC ELEMENTS CONTRIBUTING TO CELL DELAY
(NAND2 WITH FANOUT=2)

FIG. 6A



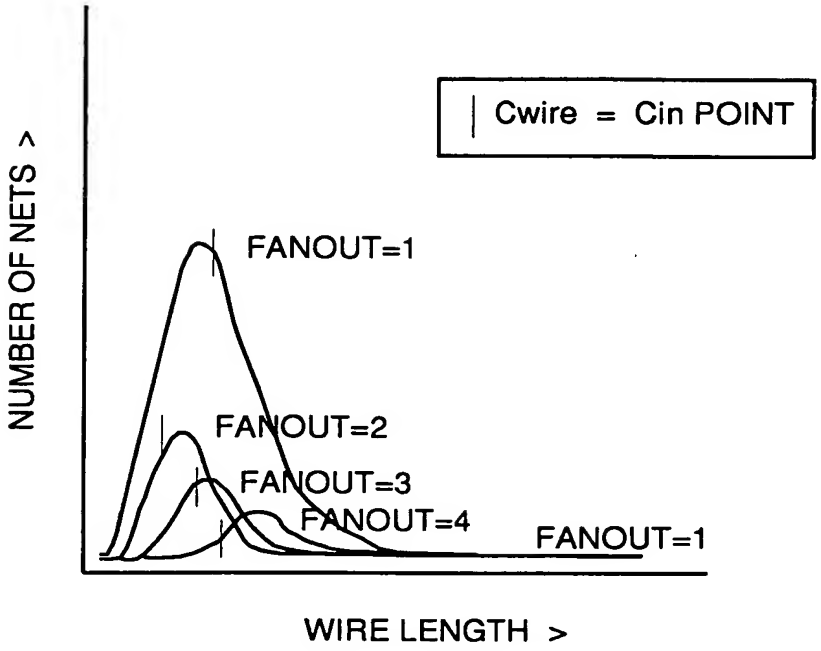
DELAY OF A NAND2 COMPONENT AS A
FUNCTION OF Cin MULTIPLIES

FIG. 6B

TECHNOLOGY NODE	Cin (pf)	LENGTH (um)
	AVERAGE	Cwire=Cin
CMOS 90nm	0.0025	6.02
CMOS 0.13um	0.0052	23.99
CMOS 0.18um	0.0079	40.63
CMOS 0.25um	0.0154	104.84

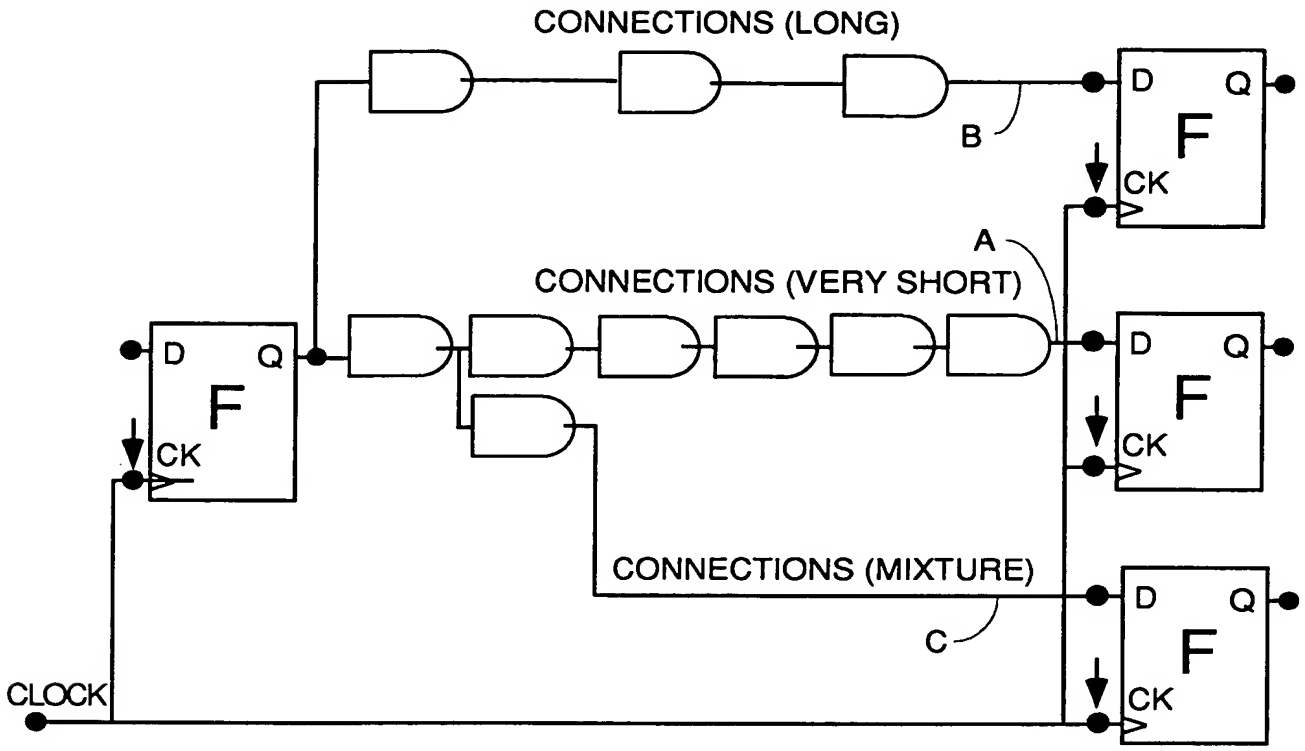
CONNECTION LENGTH WHERE Cwire
MATCHES Cin AS FUNCTION OF PROCESS

FIG. 7



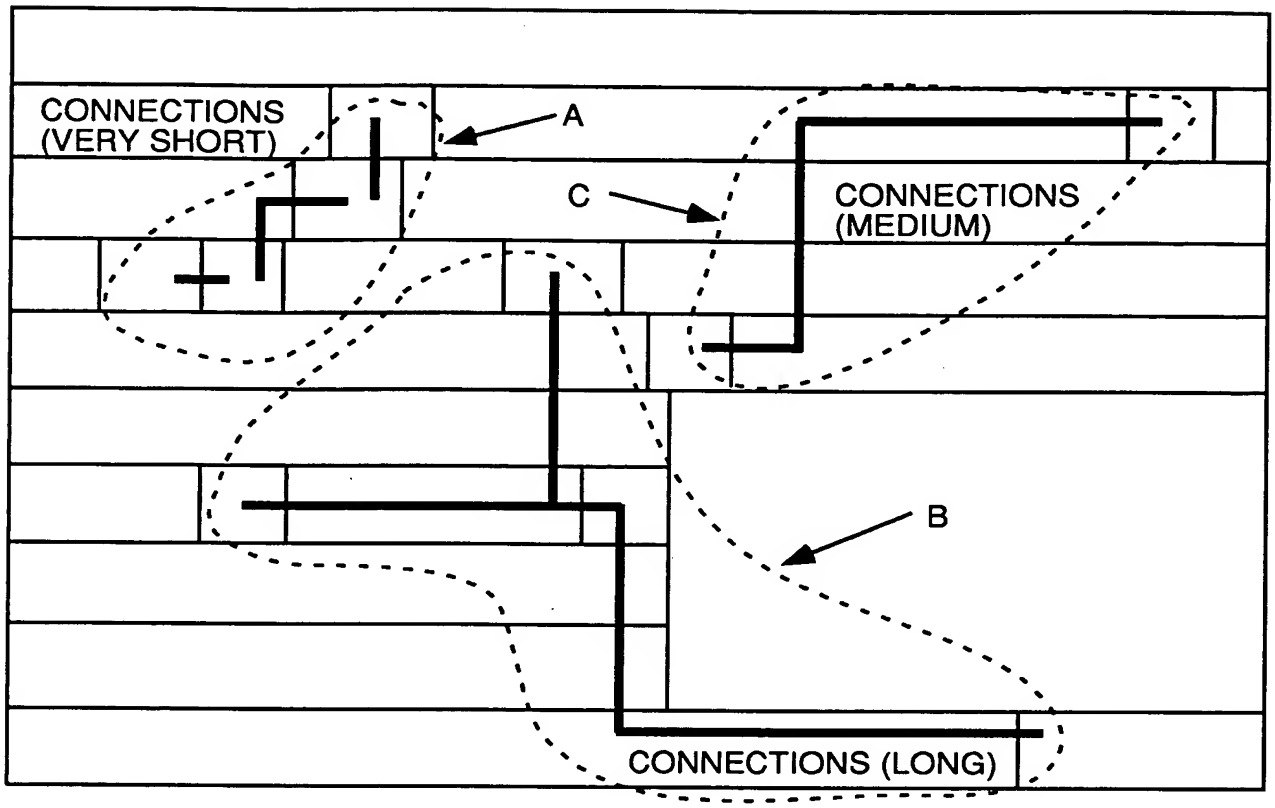
DISTRIBUTION OF CONNECTION LENGTHS BY FANOUT IN A TYPICAL CIRCUIT

FIG. 8



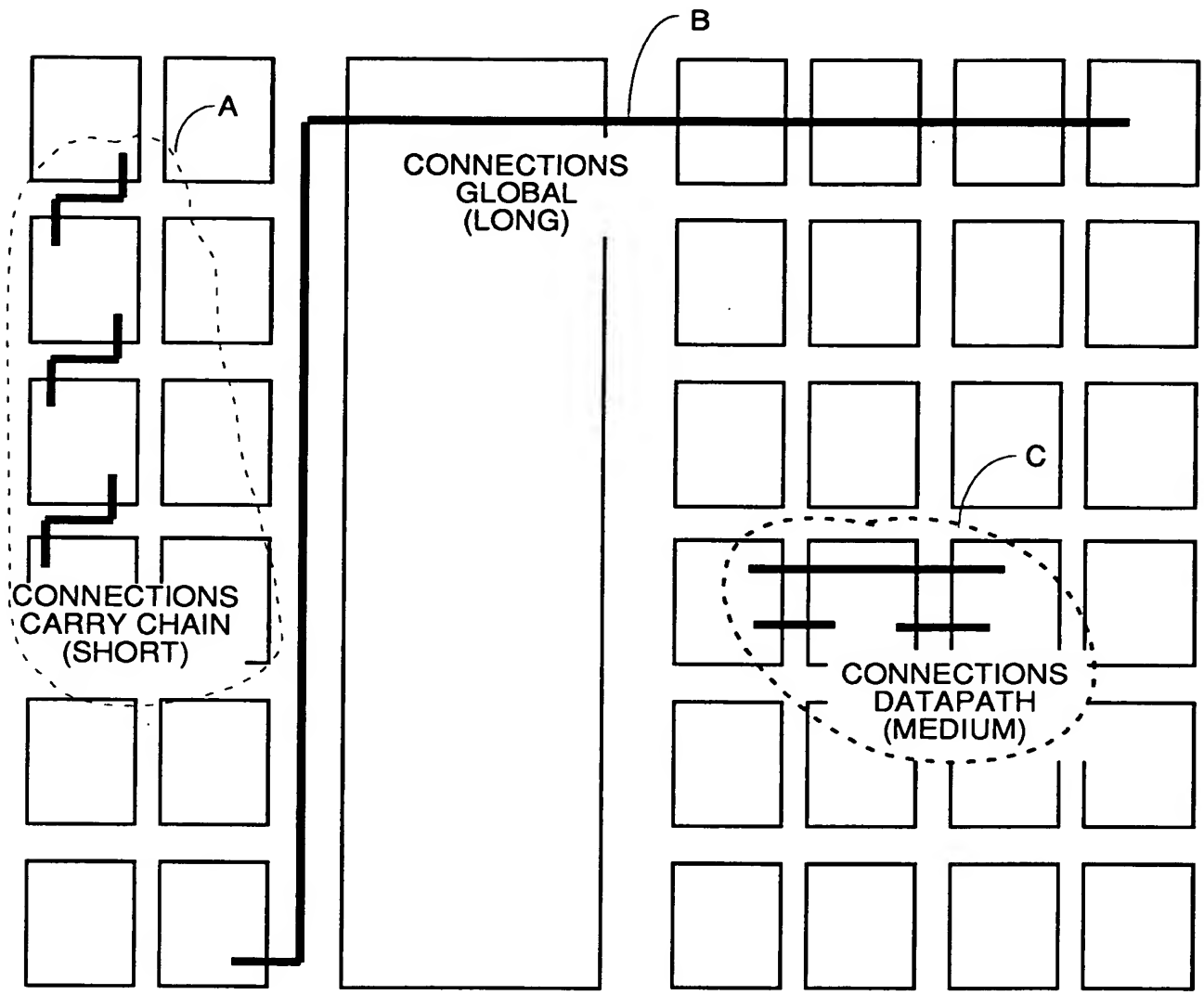
SYMBOLIC REPRESENTATION OF CRITICAL PATHS THAT CAN HAVE DIFFERENT CONNECTION LENGTHS AND MEET TIMING

FIG. 9



TYPICAL STANDARD CELL ROW LAYOUT
WITH SHORT AND LONG CONNECTIONS

FIG. 10



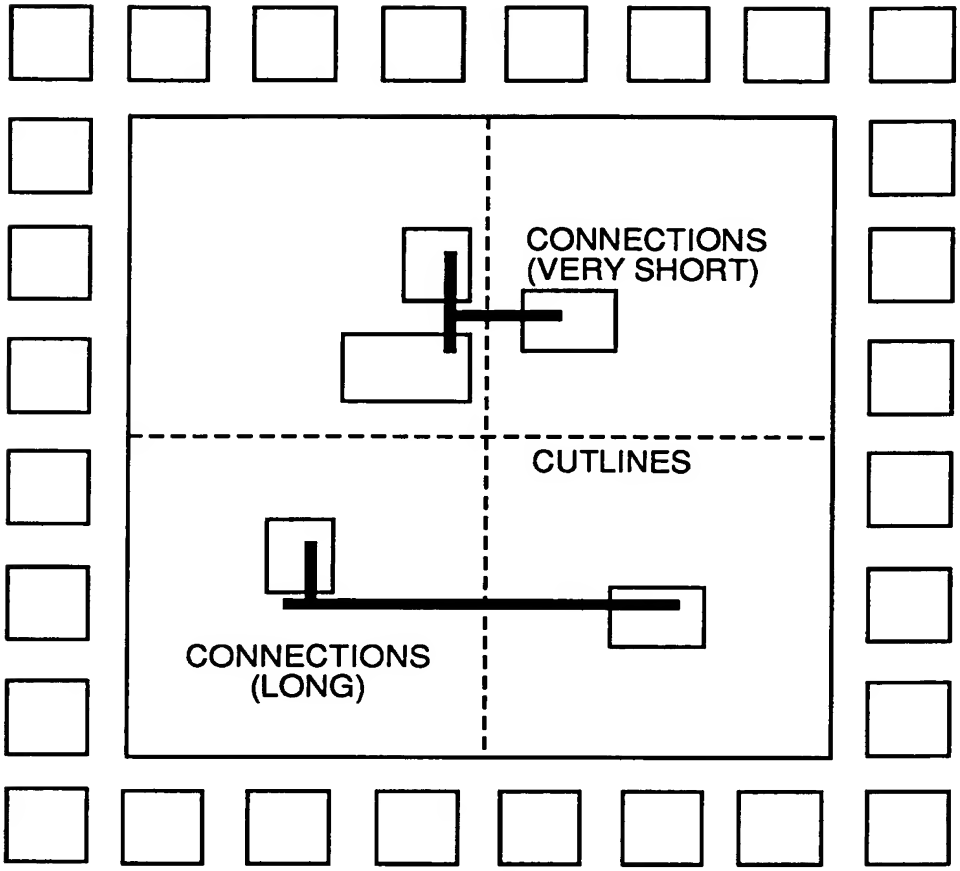
TYPICAL FIELD PROGRAMMABLE GATE ARRAY CONNECTIONS WITH SPECIAL SHORT AND LONG CONNECTIONS

FIG. 11

CONNECTION LENGTH	PARASITIC	Cin	HIERARCHY	PHYSICAL
(UM)	(SIMPLE CAP)	MULTIPLE	CLASS	WEIGHT
2.00	0.0007	0.1	SIMPLE	90
6.00	0.0021	0.4	SIMPLE	80
14.00	0.0050	1.0	SIMPLE	72
24.00	0.0086	1.7	SIMPLE	44
56.00	0.0200	4.0	SIMPLE	22
56.00	0.0200	4.0	COMPLEX	10
148.00	0.0529	10.6	SIMPLE	16
467.00	0.1668	33.4	SIMPLE	8
800.00	0.2857	57.1	SIMPLE	4
800.00	0.2857	57.1	COMPLEX	2

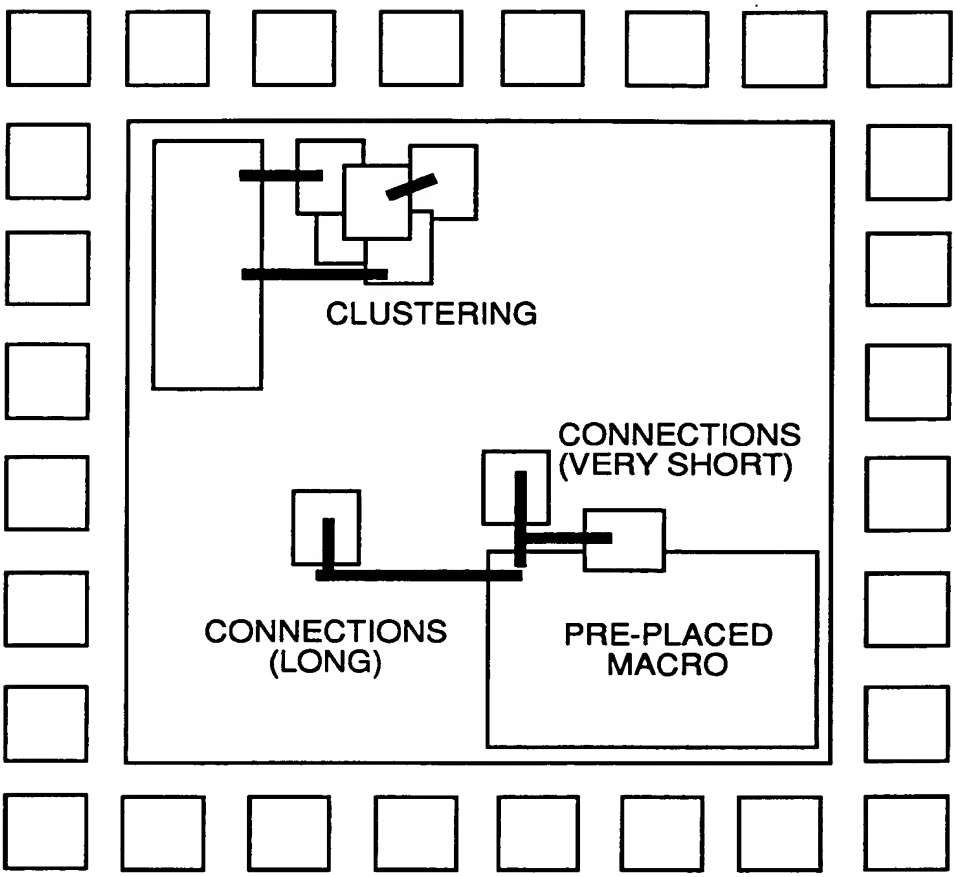
CONNECTION LENGTH FROM A PARASITIC BUDGET
TRANSLATION TO WEIGHTS FOR PLACEMENT AND PARTITIONING

FIG. 12



CONNECTION LENGTH CLUSTERING AROUND
A PLACEMENT OR PARTITIONING CUTLINE

FIG. 13



PLACEMENT CLUSTERING BASED ON
CONNECTION LENGTH FROM A PARASITIC BUDGET

FIG. 14